一众显示科技有限公司

TEAM SOURCE DISPLAY TECH. CO, LTD.

TFT-LCD Module Specification

Module NO.: TST080IA-15A

Version: V1.0

☐ APPROVAL FOR SPECIFICATION ☐ APPROVAL FOR SAMPLE

For Customer's Acceptance:	
Approved by	**Comment**

Team Source Display:		
Presented by	**Reviewed by**	**Approved by**

Version No.	Date	Content	Remark
V1.0	2023-04-21	Initial Release	

Contents

1. General Specifications

No.	Item	Specification	Remark
1	LCD Size	8 inch (Diagonal)	
2	Driver Element	a-Si TFT Active Matrix	
3	Resolution	800 x 3(RGB) x 480	
4	Display Mode	Normally Black, Transmissive, AAS	
5	Dot Pitch	72.5um(W) x 217.5um(L)	
6	Active Area	174mm(H) x 104.4mm(V)	
7	Module Size	187.4mm(W) x 118mm(H) x 6.3mm(D)	Note 1-1
8	Bezel Opening Size	177.2mm(W) x 107.4mm(H)	
9	Surface Treatment	Anti-Glare	
10	Color Arrangement	RGB-Stripe	
11	Interface	LVDS	Note 1-2
12	Backlight Power Consumption	4.32 W (Typ.)/ 4.6 W(Max)	
13	Panel Power Consumption(mW)	660mW(Typ)	
14	Inversion method	Dot Inversion	
15	Weight(g)	205	
16	Green	Follow RoHS	

Note 1-1: Refer to Mechanical Drawing.

Note 1-2: LVDS, 8-bit, DE mode, JEIDA/VESA format

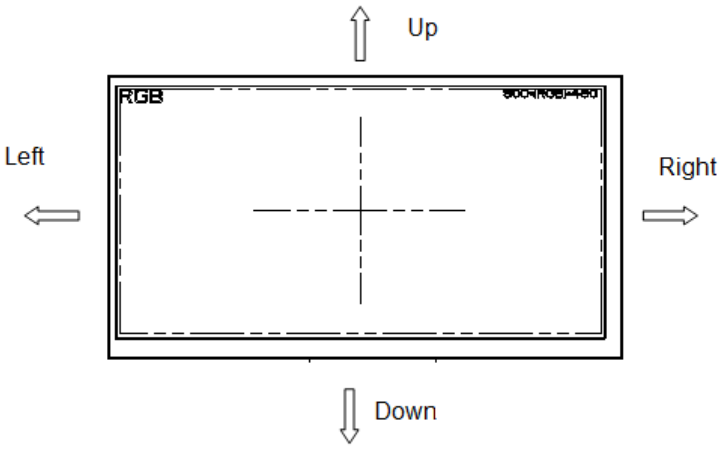
2. Pin Assignment

Main FPCa golden finger pin define			
PIN NO.	**Symbol**	**I/O/P**	**Function**
1	GND	P	Ground.
2	VDD	P	Digital power(3.3V).
3	VDD	P	Digital power(3.3V).
4	VDD	P	Digital power(3.3V).
5	GSPD	O	Gate scan down start signal (For fail safe).
6	NC(TSD OTP pin)	P	OTP power pin, please keep floating.
7	GND(TSD SDI pin)	I	Serial communication data input pin, please setting for GND.
8	NC(TSD SDO pin)	O	Serial communication data output pin, please keep floating.
9	GND(TSD SCL pin)	I	Serial communication clock input pin, please setting for GND.
10	VDD(TSD CS pin)	I	Serial communication chip selection pin, please setting for VDD.
11	SSCEN	I	SSCG enable/disable setting.
12	UD	I	Vertical scan direction.
13	STBYB(MUTE)	I	Standby mode.
14	RESET	I	Global reset pin.
15	LR	I	Horizontal scan direction.
16	LVFMT	I	VESA/JEIDA format selection pin.
17	BLKINSER	I	For DE mode skipped function, please setting for GND. Normal display using, please setting for VDD.
18	GND	P	Ground.
19	LVDS D+	I	LVDS data D+.
20	LVDS D-	I	LVDS data D-.
21	GND	P	Ground.
22	LVDS CLK+	I	LVDS CLK+.
23	LVDS CLK-	I	LVDS CLK-.
24	GND	P	Ground.
25	LVDS C+	I	LVDS data C+.
26	LVDS C-	I	LVDS data C-.
27	GND	P	Ground.
28	LVDS B+	I	LVDS data B+.
29	LVDS B-	I	LVDS data B-.
30	GND	P	Ground.
31	LVDS A+	I	LVDS data A+.
32	LVDS A-	I	LVDS data A-.
33	GND	P	Ground.
34	GND(TSD test pin)	P	TSD test pin(BISTEN), please setting for GND.
35	LED1-	P	Negative backlight voltage.

36	LED2-	P	Negative backlight voltage.
37	LED3-	P	Negative backlight voltage.
38	NC	P	Keep floating.
39	LED+	P	Positive backlight voltage.
40	LED+	P	Positive backlight voltage.

LR	UD	Data shifting
VDD	VDD	Left→Right，UP→Down(default)
VDD	GND	Left→Right，Down→UP
GND	VDD	Right→Left，UP→Down
GND	GND	Right→Left，Down→UP

Refer to the figure as below:



LVFMT	VESA/JEIDA format
H(default)	VESA Format.
L	JEIDA Format.

SSCEN	Enable/Disable
H	Enable
L(default)	Disable

3. Operating Specifications

3.1 Absolute Maximum Rating

(GND=0V, TJ=25℃,Note 1)

Item	Symbol	Values		Unit	Remark
		Min.	Max.		
Power Voltage	VDD	-0.3	5	V	Note 1
Storage Temperature	TST	-40	+95	ºC	Note 2
Operating Ambient Temperature	TOP	-30	+85	ºC	Note 2

Note 1: The absolute maximum rating values of this product are not allowed to be exceeded at any times. Should a module be used with any of the absolute maximum ratings exceeded, the characteristics of the module may not be recovered, or in an extreme case, the module may be permanently destroyed.

Note 2: Condensation of dew must be avoided as electrical current leaks will occur. Causing a degradation of performance specifications.

3.1.1 Typical Operation Conditions

item	Symbol	Min.	Typ.	Max.	Unit.	Note.
Digital Supply Voltage	VDD	3	3.3	3.6	V	Note 3-1、Note 3-3
Digital Supply Current	I_{VDD}	-	230	300	mA	Note 3-2
Logic Input Voltage	VIH	0.7VDD	-	VDD	V	Note 3-3
	VIL	GND	-	0.3VDD	V	
Logic Output Voltage	VOH	VDD-0.4	-	VDD	V	Note 3-4
	VOL	GND	-	GND+0.4	V	
Output Current	**Io**	-	1	-	mA	Note 3-5

Note 3-1: VDD setting should match the signals output voltage of customer's system board

Note 3-2: I_{VDD} is full white pattern, Condition: VDD=3.3V

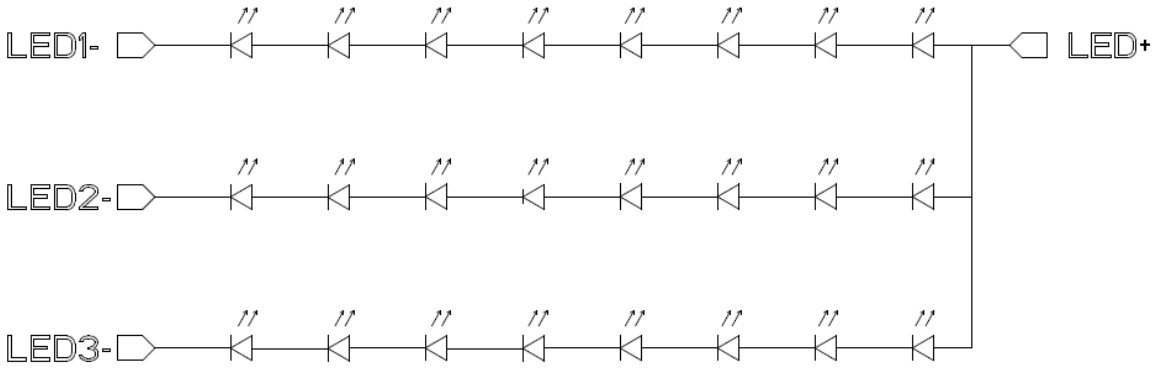
Note 3-3: LR, RESET, STBYB, UD, LVFMT, BLINKSER, SSCEN.

Note 3-4: GSPD

Note 3-5: Based on output voltage level (VOH&VOL)

3.1.2 Backlight Driving Conditions

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Voltage for LED Backlight	VL	22.4	24.8	26.4	V	Note 3-3
Current for LED Backlight	I_L		174		mA	
LED Life Time	-	10000			Hr	Note 3-4
LED Life Time(Ta=85℃)		6000			Hr	Note 3-5



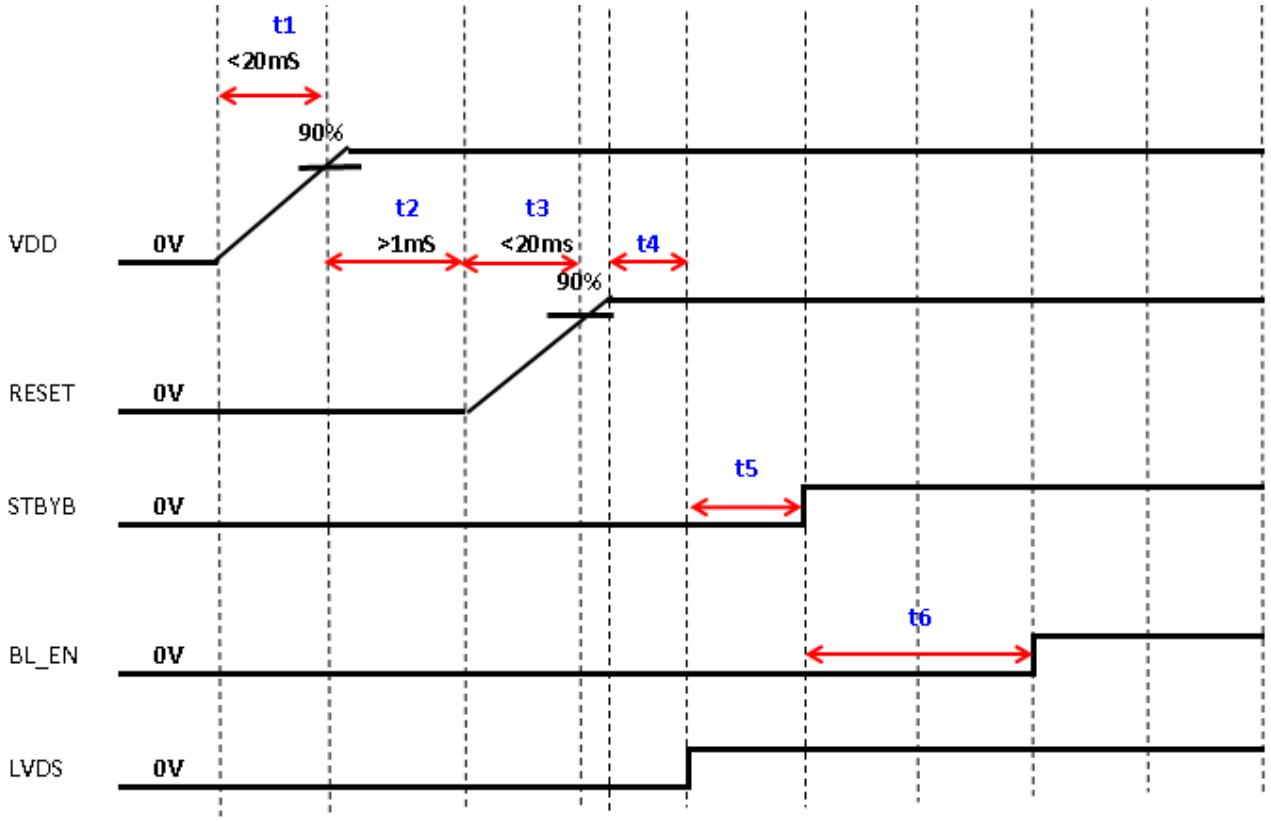
Note 3-3: The LED Supply Voltage is defined by the number of LED at Ta=25℃ and I_L =450mA.

Note 3-4: The "LED life time" is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and I_L = 450mA. The LED lifetime could be decreased if operating I_L is larger than 450mA

Note 3-5: The "LED life time" is defined as the module brightness decrease to 50% original brightness at Ta=85℃ and I_L = 450mA. The LED lifetime could be decreased if operating I_L is larger than 450mA.

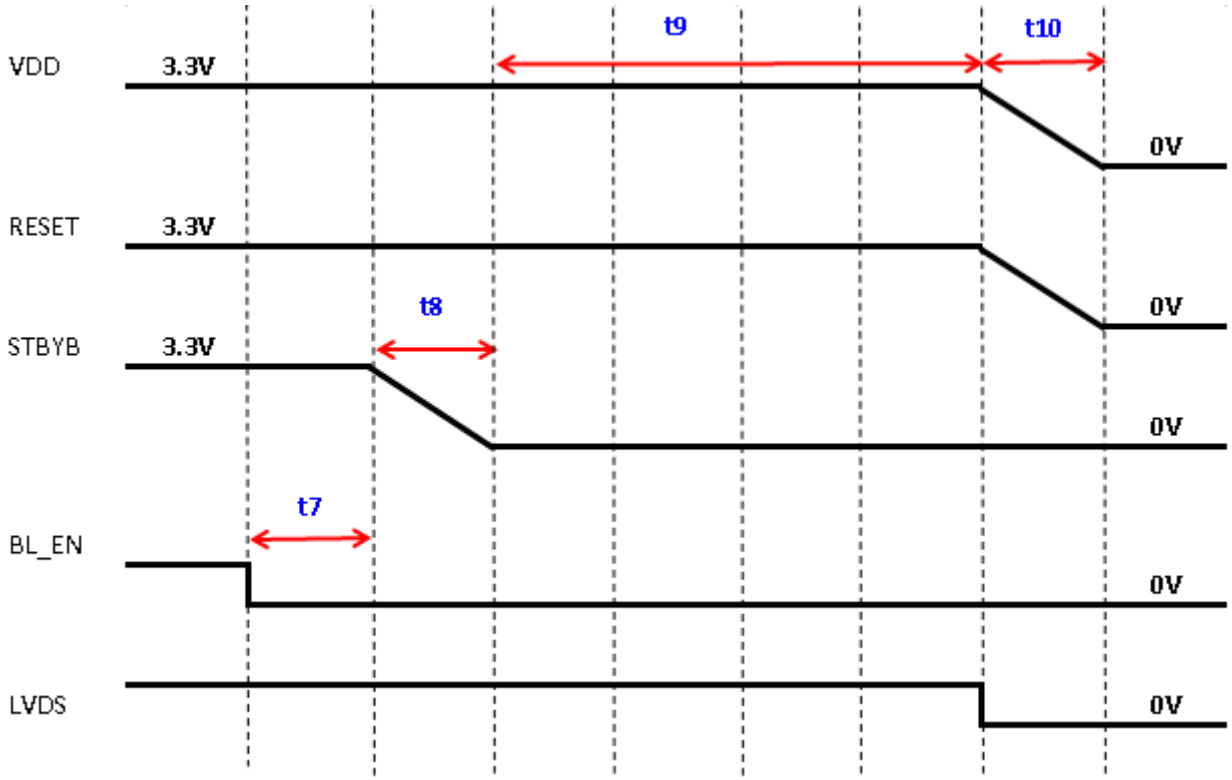
3.2 Power Sequence

Power on sequence:



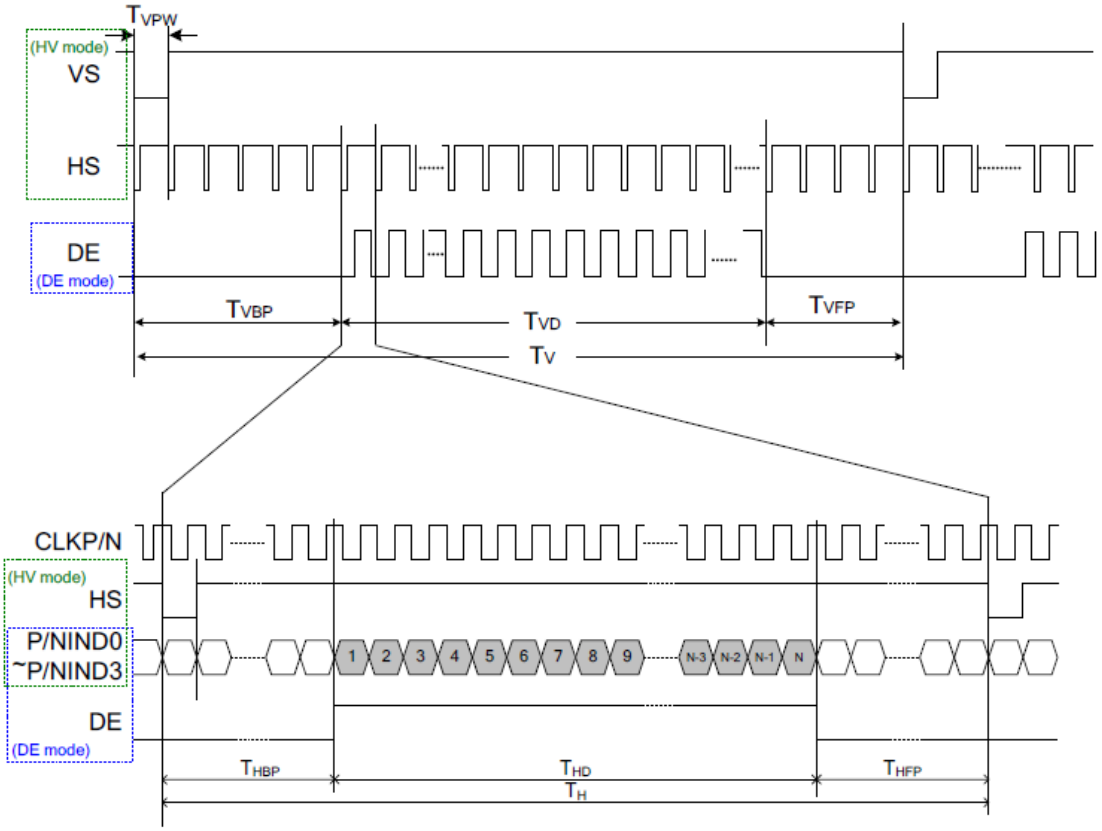
Symbol	SPEC.			Unit
	Min.	Typ.	Max.	
t1	0	5	20	ms
t2	1	3	50	ms
t3	0	5	20	ms
t4	1	3	500	ms
t5	2	5	50	ms
t6	170	180	5000	ms

Power off sequence:



Symbol	SPEC.			Unit
	Min.	Typ.	Max.	
t7	10	20	50	ms
t8	0	2	10	ms
t9	170	180	250	ms
t10	0	2	150	ms

3.3 LVDS Input Timing



Note:
$T_V=T_{VBP}+T_{VD}+T_{VFP}$
$T_H=T_{HBP}+T_{HD}+T_{HFP}$

Figure 3-1. LVDS Input Timing

DE mode for 800x480 normal setting

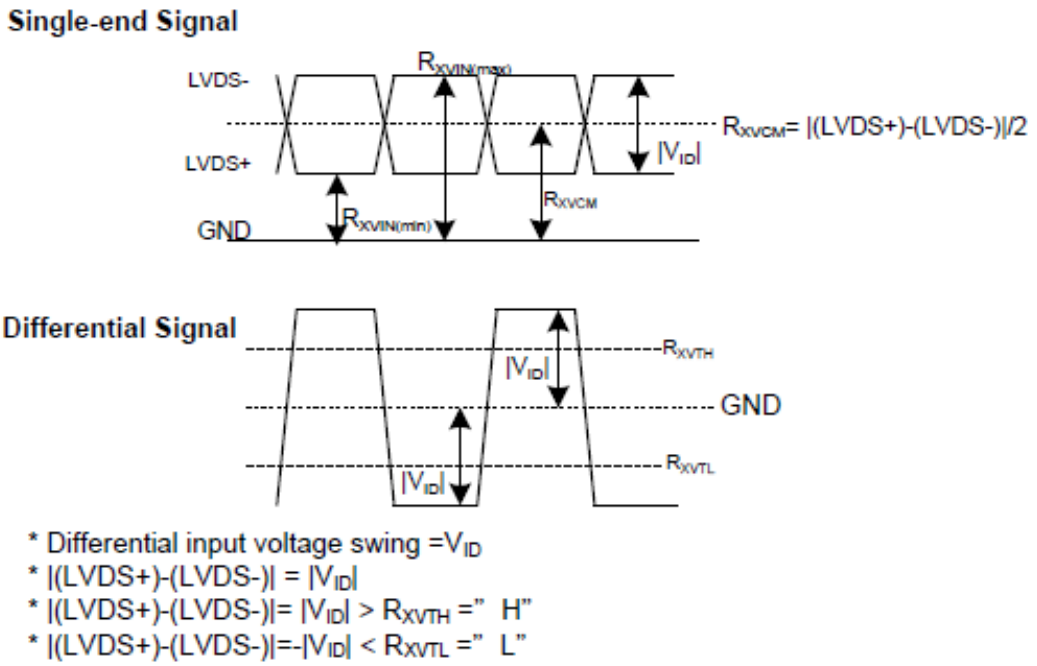
Parameter	Symbol	Min.	Typ.	Max.	Unit
CLK frequency	F_{CLK}	25.2	25.4	37.2	MHz
Horizontal display area	T_{HD}		800		CLK
HS period time	T_H	860	864	1110	CLK
HS blanking	$T_{HFP}+T_{HBP}$	60	64	310	CLK
Vertical display area	T_{VD}		480		H
VS period time	T_V	488	490	560	H
VS blanking	$T_{VBP}+T_{VFP}$	8	10	80	H
Frame rate	-	60.0457	59.9962	59.8455	Hz

37MHz clock reference setting

Parameter	Symbol	Min.	Typ1.	Typ2.	Max.	Unit
CLK frequency	F_{CLK}	36.6240	36.8640	36.9524	37.2960	MHz
Horizontal display area	T_{HD}		800			CLK
HS period time	T_H	1090	1097	1097	1110	CLK
HS blanking	$T_{HFP}+T_{HBP}$	290	297	297	310	CLK
Vertical display area	T_{VD}		480			H
VS period time	T_V	560	560	560	560	H
VS blanking	$T_{VBP}+T_{VFP}$	80	80	80	80	H
Frame rate	-	60	60.0078	60.1517	60	Hz

3.3.1 LVDS DC Interface Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Differential input high threshold voltage	R_{XVTH}	+0.1	-	-	V	R_{XVCM}=1.2V
Differential input low threshold voltage	R_{XVTL}	-	-	-0.1	V	
Input voltage range (singled-end)	R_{XVIN}	0.7	-	1.7	V	
Differential input common Mode voltage	R_{XVCM}	1	1.2	1.4	V	
Differential input voltage	$\|V_{ID}\|$	0.2	-	0.6	V	
Terminal resistor	R_{TERM}	-	100	-	Ω	
Differential input leakage current	I_{LLVDS}	-10	-	+10	uA	VDD_IF=3.3V, CLKP/N, DxP/N
LVDS Digital Stand-by Current	I_{STLVDS}	-	-	100	uA	VDD_IF=3.3V, Input Pin V_{IH} =3.3V, V_{IL} =0V, Clock & all functions are stopped, STBYB = L
LVDS Digital Operating Current	$I_{VDDLVDS}$	-	-	60	mA	VDD_IF=3.3V, Input Pin V_{IH} =3.3V, V_{IL}=0V, F_{CLK} =85MHz, Input pattern: 55h->AAh->55h->AAh



* Differential input voltage swing =V_{ID}
* |(LVDS+)-(LVDS-)| = $|V_{ID}|$
* |(LVDS+)-(LVDS-)|= $|V_{ID}| > R_{XVTH}$ =" H"
* |(LVDS+)-(LVDS-)|=-$|V_{ID}| < R_{XVTL}$ =" L"

Figure 3-2. LVDS DC Diagram

3.3.2 LVDS Interface AC Electrical Characteristic

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Clock frequency	F_{LVCLK}	20	-	85	MHz	Refer to input timing table for each display resolution.
Clock Period	T_{LVCLK}	50	-	11.76	nsec	
Clock high time	T_{LVCH}	-	4/(7* R_{XFCLK})	-	ns	
Clock low time	T_{LVCL}	-	3/(7* R_{XFCLK})	-	ns	
Input data skew margin	T_{RSKM}	-	-	0.2	UI	|VID | = 200mV, R_{XVCM} = 1.2V F_{LVCLK} =36.624~37.296MHz
Strobe width	T_{SW}	0.6	-	-	UI	
1 data bit time	UI		1/7		T_{LVCLK}	
Position 1	T_{POS1}	-0.2	0	0.2	UI	
Position 0	T_{POS0}	0.8	1	1.2	UI	
Position 6	T_{POS6}	1.8	2	2.2	UI	
Position 5	T_{POS5}	2.8	3	3.2	UI	
Position 4	T_{POS4}	3.8	4	4.2	UI	
Position 3	T_{POS3}	4.8	5	5.2	UI	
Position 2	T_{POS2}	5.8	6	6.2	UI	
PLL wake-up time	T_{enPLL}	-	-	150	us	
SSC Modulation Frequency	SSC_{MF}	23	-	93	KHz	
SSC Modulation Rate	SSC_{MR}	-3	-	+3	%	F_{LVCLK} =81MHz, Center spread

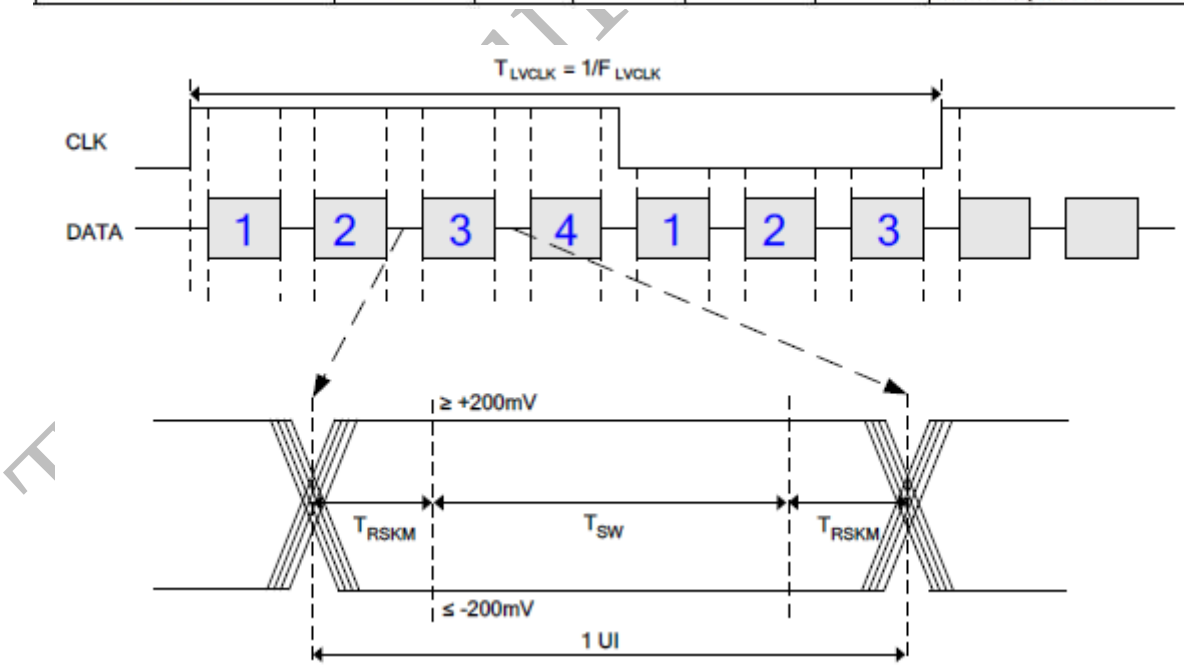


Figure 3-3 . LVDS Data Skew

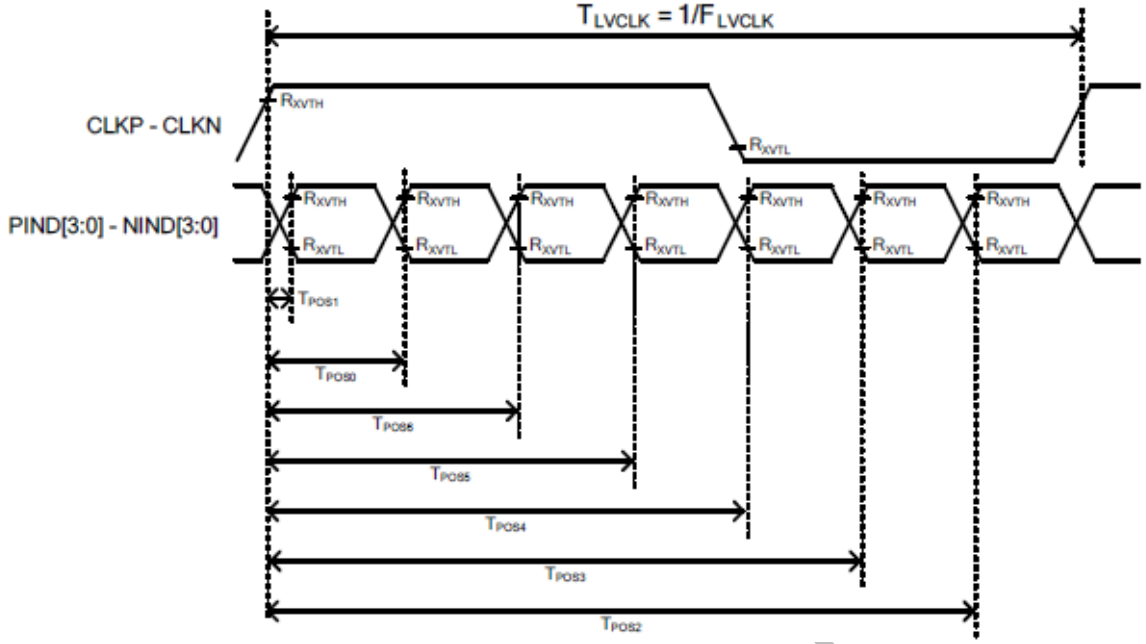


Figure 3-4. LVDS input timing

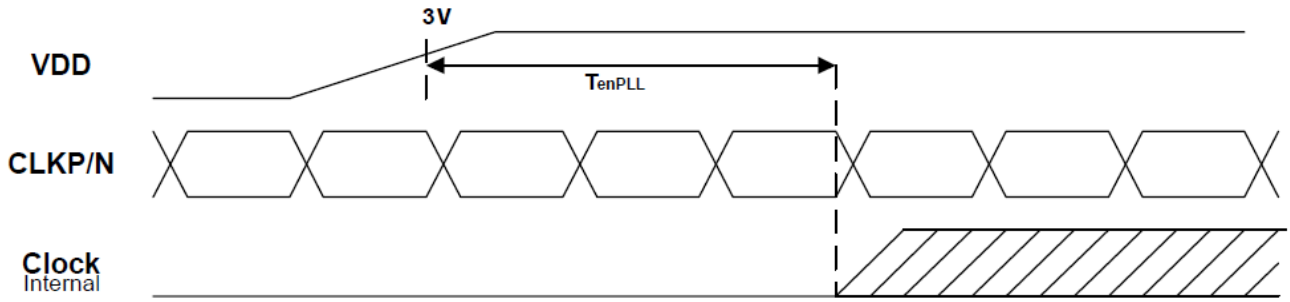


Figure 3-5. Relationship between VDD, LVDS clock, and internal clock

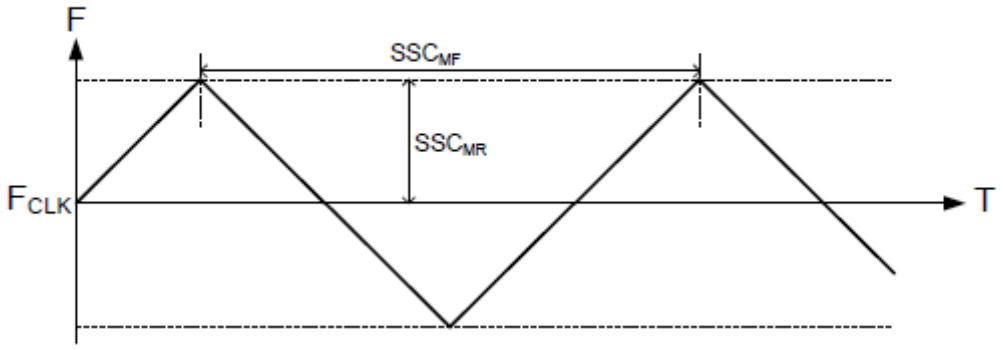


Figure 3-6. Frequency Modulation

3.3.3 Data Input JEIDA Format for LVDS

LVDS, 8-bit, JEIDA format

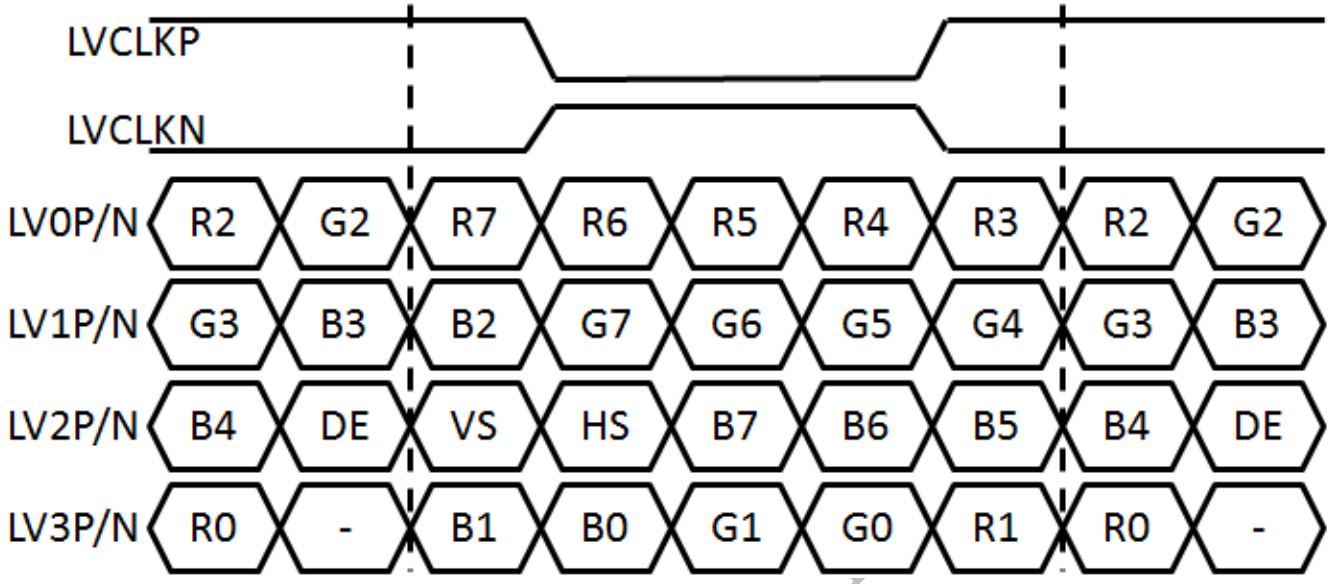


Figure 3-7. 8-bit LVDS Input(JEIDA format)

3.3.4 Data Input VESA Format for LVDS

LVDS, 8-bit, VESA format

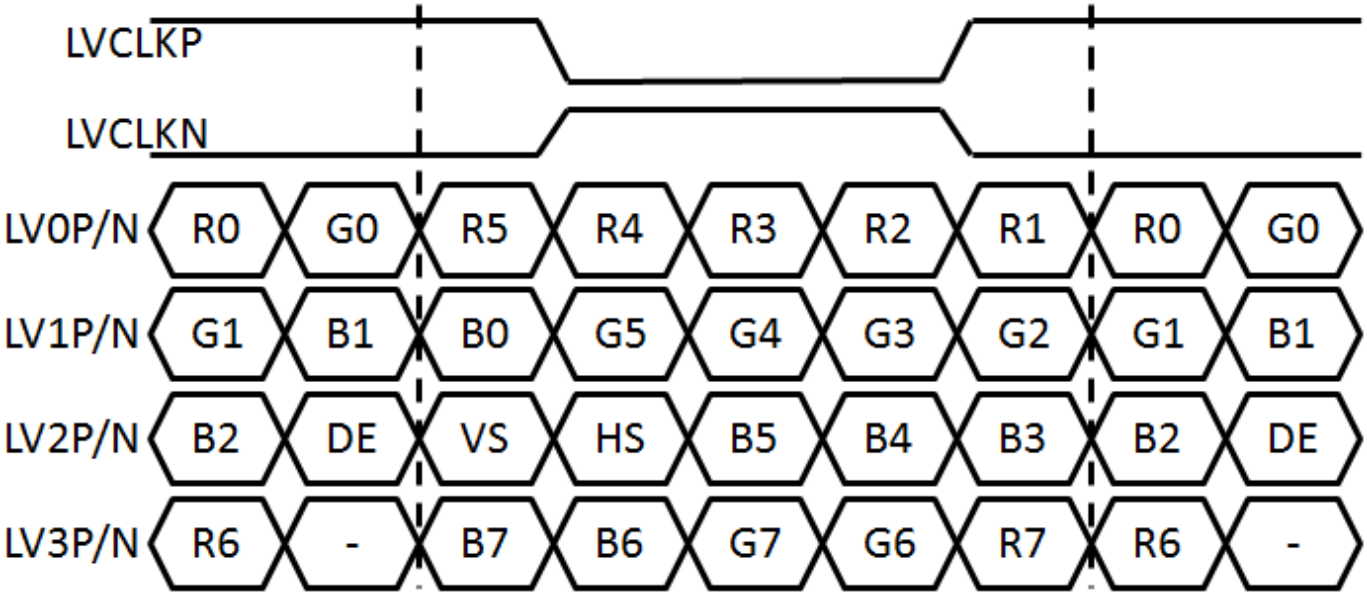


Figure 3-8. 8-bit LVDS Input(VESA format)

3.3.5 SSCG function

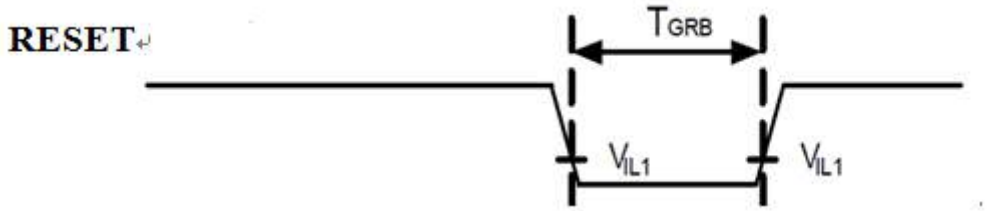
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
SSCG Modulation rate	-	-0.075	-|	+0.075	%	Pin 11_SSCEN enable
SSCG Modulation frequency	-	-	1.4		MHz	Pin 11_SSCEN enable

Note: SSCG is spread the IC internal signal, RX to TCON

3.3.6 AC timing

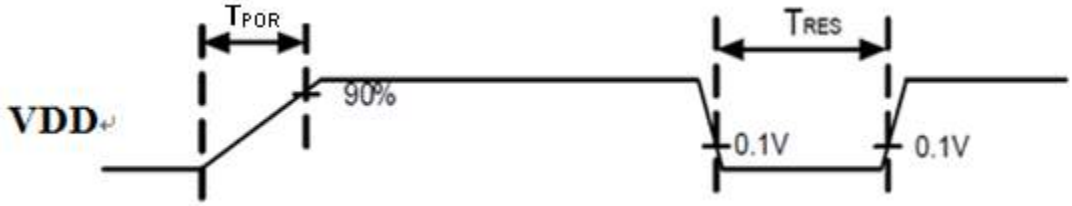
Reset:

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Reset active pulse width	T_{GRB}	1	-	-	ms	VDD=3.3V , V_{IL1}=30%



VDD:

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
VDD power source slew time	T_{POR}	-	-	20	ms	From 0V to 90% VDD
VDD resettle time	T_{RES}	100	-	-	ms	VDD repower on delay time.



4. Optical Specifications

Item	Symbol	Condition	Values			Unit	Remark
			Min.	Typ.	Max.		
Viewing Angle (CR≥10)	θ_L	Φ=180°(9 o'clock)	80		-	degree	Note 4-1
	θ_R	Φ=0°(3 o'clock)	80		-		
	θ_T	Φ=90°(12 o'clock)	80		-		
	θ_B	Φ=270°(6 o'clock)	80		-		
Response Time(W<-->B)	Ton+Toff @25℃	Normal θ=Φ=0°	-	25	30	msec	Note 4-3
	Ton+Toff @-20℃		-	-	250		
Contrast Ratio	CR		800	1000	-	-	Note 4-4
Color Chromaticity	W_X		0.270	0.310	0.350	-	Note 4-2 Note 4-5 Note 4-6
	W_Y		0.290	0.330	0.370	-	
	R_X		0.606	0.646	0.686		
	R_Y		0.299	0.339	0.379		
	G_X		0.267	0.307	0.347		
	G_Y		0.563	0.603	0.643		
	B_X		0.109	0.149	0.189		
	B_Y		0.015	0.055	0.095		
NTSC (CIE1931)	-			70		%	Note 4-5
Luminance (Center)	L		740	920	-	cd/m²	Note 4-6
Luminance (Center) H ±30°& V±-5°	L		550	700		cd/m²	Note 4-6
Luminance Uniformity	Y_U		75	-	-	%	Note 4-7
Flicker					8	%	Note 4-8

Test Conditions:

1. **VDD=3.3V, I_L=174mA (Backlight current), the ambient temperature is 25℃**
2. **The test systems refer to Note 2.**

Note 4-1: Definition of viewing angle range

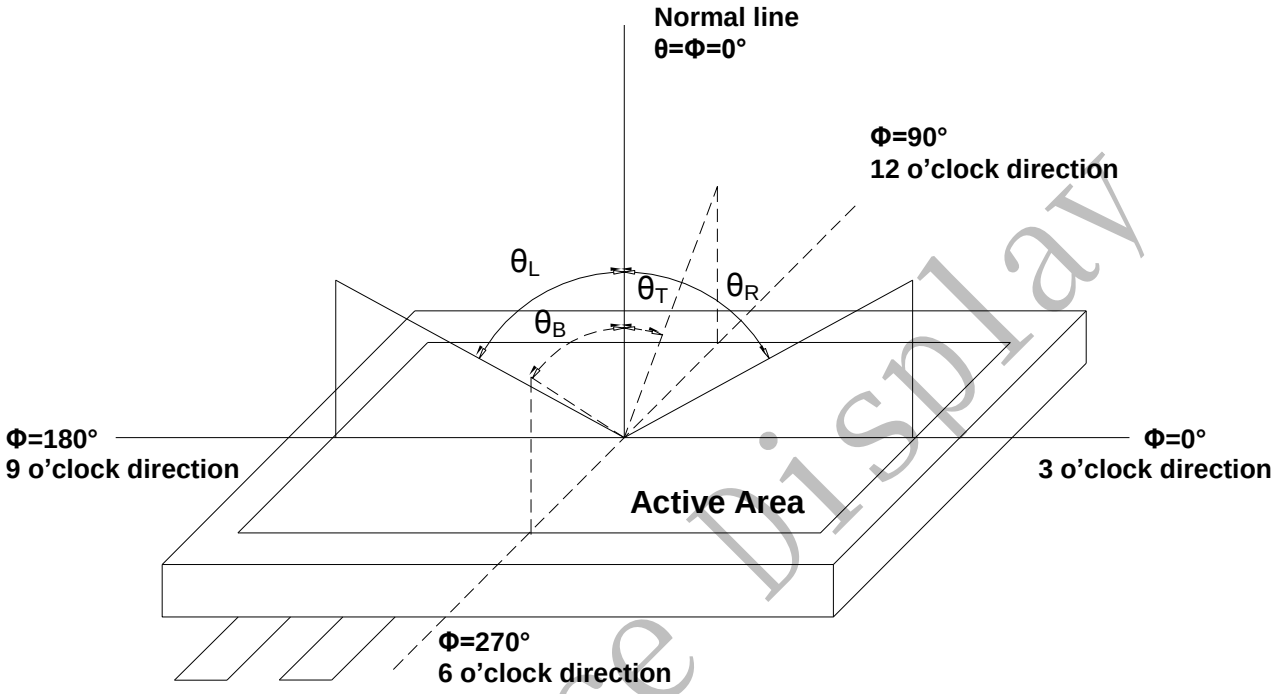


Fig. 4-1 Definition of viewing angle

Note 4-2: Definition of optical measurement system.

The optical characteristics should be measured in dark room. The optical properties are measured at the center point of the LCD screen.

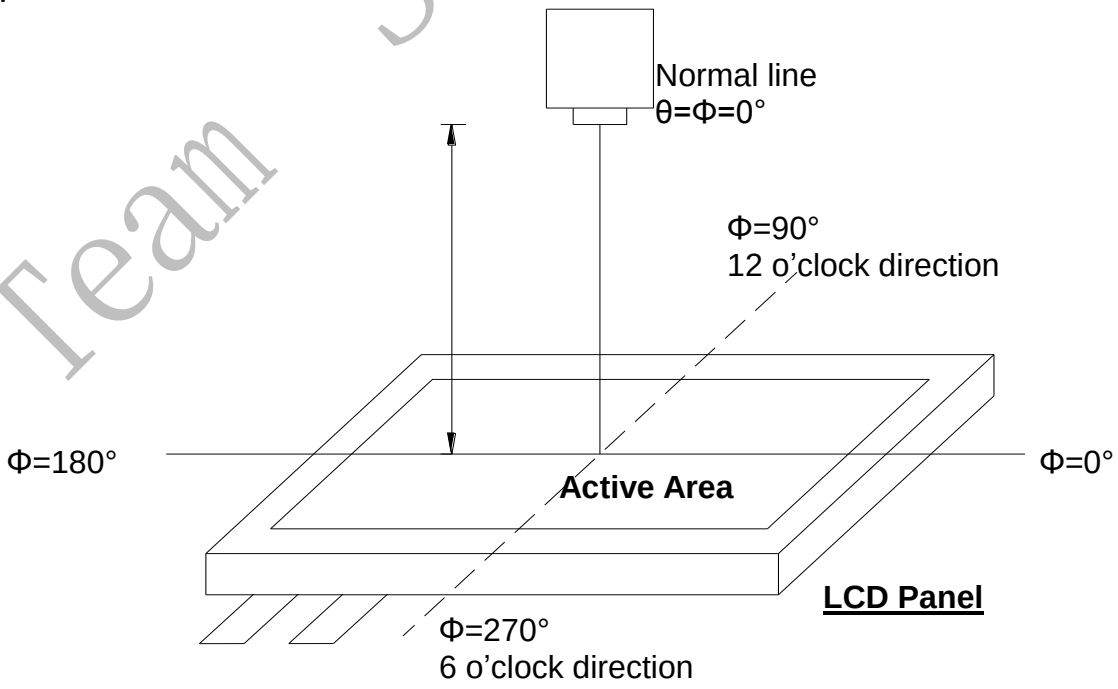


Fig. 4-2 Optical measurement system setup

Note 4-3: Definition of Response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state.

Rise time (T_{ON}) is the time between photo detector output intensity changed from 10% to 90%.

And fall time (T_{OFF}) is the time between photo detector output intensity changed from 90% to 10%.

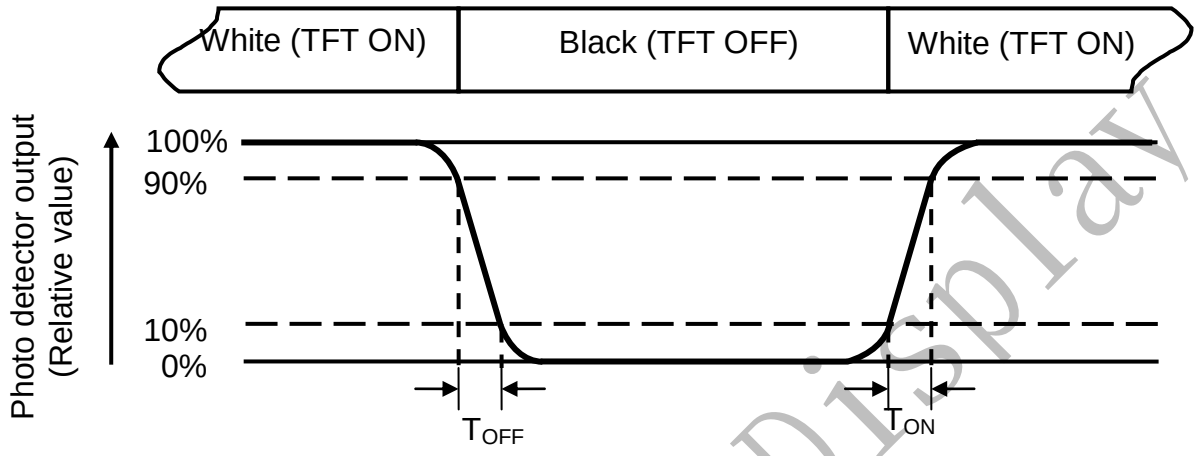


Fig. 4-3 Definition of response time

Note 4-4: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 4-5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

Note 4-6: All input terminals LCD panel must be ground while measuring the center area of the panel. The LED BLU driving condition is I_L= 174mA. Operate at -20°C should be light on within 3 seconds.

Note 4-7: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer to Fig. 4-4). Every measuring point is placed at the center of each measuring area.

$$Luminance Uniformity(Yu) = \frac{B_{min}}{B_{max}}$$

L-------Active area length W----- Active area width

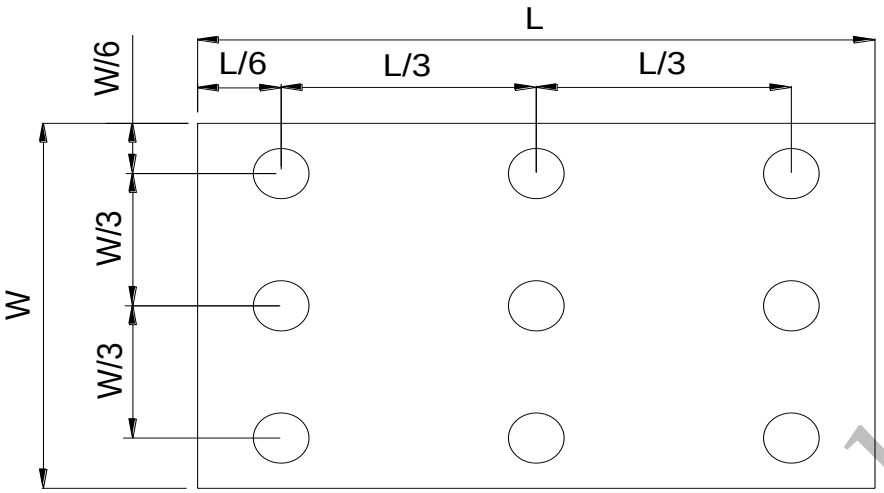


Fig. 4-4 Definition of measuring points

B_{max}: The measured maximum luminance of all measurement position.

B_{min}: The measured minimum luminance of all measurement position.

Note 4-8: Flicker

The panel is power on waiting for 75s at auto-run pattern before it is measured flicker value. Under Gray 50% pattern (L127) (Fig. 4-5) at the center point of the LCD screen by CA-210.

Fig. 4-5 Gray 50% pattern (L127)

5. Reliability Test Items

High Temperature Storage Test	Ta = 95±2ºC, 240 hours	Note 5-1 Note 5-2 Note 5-4
High Temperature Operation Test	Tp = 85±2ºC, 240 hours	
Low Temperature Operation Test	Ta = -30±3ºC, 240 hours	
Low Temperature Storage Test	Ta = -40±3ºC, 240 hours	
High Temperature & High Humidity Operation Test	65±2ºC, RH 90±2%, 240hours	
Thermal Shock	(-30℃ 30min)→(80℃ 30min)]/cycle,100 cycles	
Room Temperature Operation Test	Ta = 30±5ºC, 10000 hours	
ESD Test	C = 150pF, R = 330Ω, Air Discharge, ± 15KV, Class B	Note 5-1
Mechanical Shock	100G, 6ms, half sine wave, 3 times for each direction of ±X, ±Y, ±Z	Note 5-1 Note 5-3
Mechanical Vibration	5 to 10 Hz, Amplitude 25 mm 10 to 30 Hz, 3.7 × 9.8 m / s 2 30 to 50 Hz, 1.6 × 9.8 m / s 2 50 to 80 Hz, 0.7 × 9.8 m / s 2 80 to 200 Hz, 0.3 × 9.8 m / s 2 X, Y, Z direction 8 min × 2 sweep Each direction 96 hours	Note 5-1 Note 5-3
Packaging Vibration Test	1.14Grms X, Y, Z three axes (30min /axis) [Frequency：5Hz(0.015G2/Hz)，100Hz(0.015G2/Hz)， 200Hz(0.0037G2/Hz)]	
Packaging Drop Test	1corner, 3edges, 6faces (1 time/direction) <follow ISTA(1A) height> 0kg≦W <10kg：76cm, 10kg≦W <19kg：61cm, 19kg≦W <28kg：46cm, 28kg≦W <45kg：31cm, 45kg≦W ≦68kg：20cm	

Ta = Ambient Temperature Tp = Panel Surface Temperature

Note 5-1 Criteria : Normal display image with no obvious non-uniformity and no line defect.

Note 5-2 Evaluation should be tested after storage at room temperature for more than two hour

Note 5-3 At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

Note 5-4 A certain level of Mura (non-uniformity) of dark / black image will happen several days after high temperature testing (H.T.T.). There is a slowly part recovery over a long time (several months). Such a long exposure time like in H.T.T. will normally not happen in a real application. Therefore the test H.T.T. was introduced to simulate cycles with normal conditions in-between but with the same total exposure time what show a significant reduced Mura. The root cause is related to tension generated due to different amount of shrinking in the stack of layers in the polarizer sheet. The effect is more significant on larger displays like this size. An investigation into alternative polarizer material showed that there is no better alternative currently available.

6. General Precautions

6.1 Safety

Liquid crystal is poisonous. Do not put it in your mouth. If liquid crystal touches your skin or clothes, wash it off immediately by using soap and water.

6.2 Handling

1. The LCD panel is plate glass. Do not subject the panel to mechanical shock or to excessive force on its surface.

2.The polarizer attached to the display is easily damaged. Please handle it carefully to avoid scratch or other damages.

3. To avoid contamination on the display surface, do not touch the module surface with bare hands.

4. Keep a space so that the LCD panels do not touch other components.

5. Put cover board such as acrylic board on the surface of LCD panel to protect panel from damages.

6. Transparent electrodes may be disconnected if you use the LCD panel under environmental conditions where the condensation of dew occurs.

7. Do not leave module in direct sunlight to avoid malfunction of the ICs.

6.3 Static Electricity

1. Be sure to ground module before turning on power or operating module.

2. Do not apply voltage which exceeds the absolute maximum rating value.

6.4 Storage

1. Store the module in a dark room where must keep at 25±10℃ and 65%RH or less.

2. Do not store the module in surroundings containing organic solvent or corrosive gas.

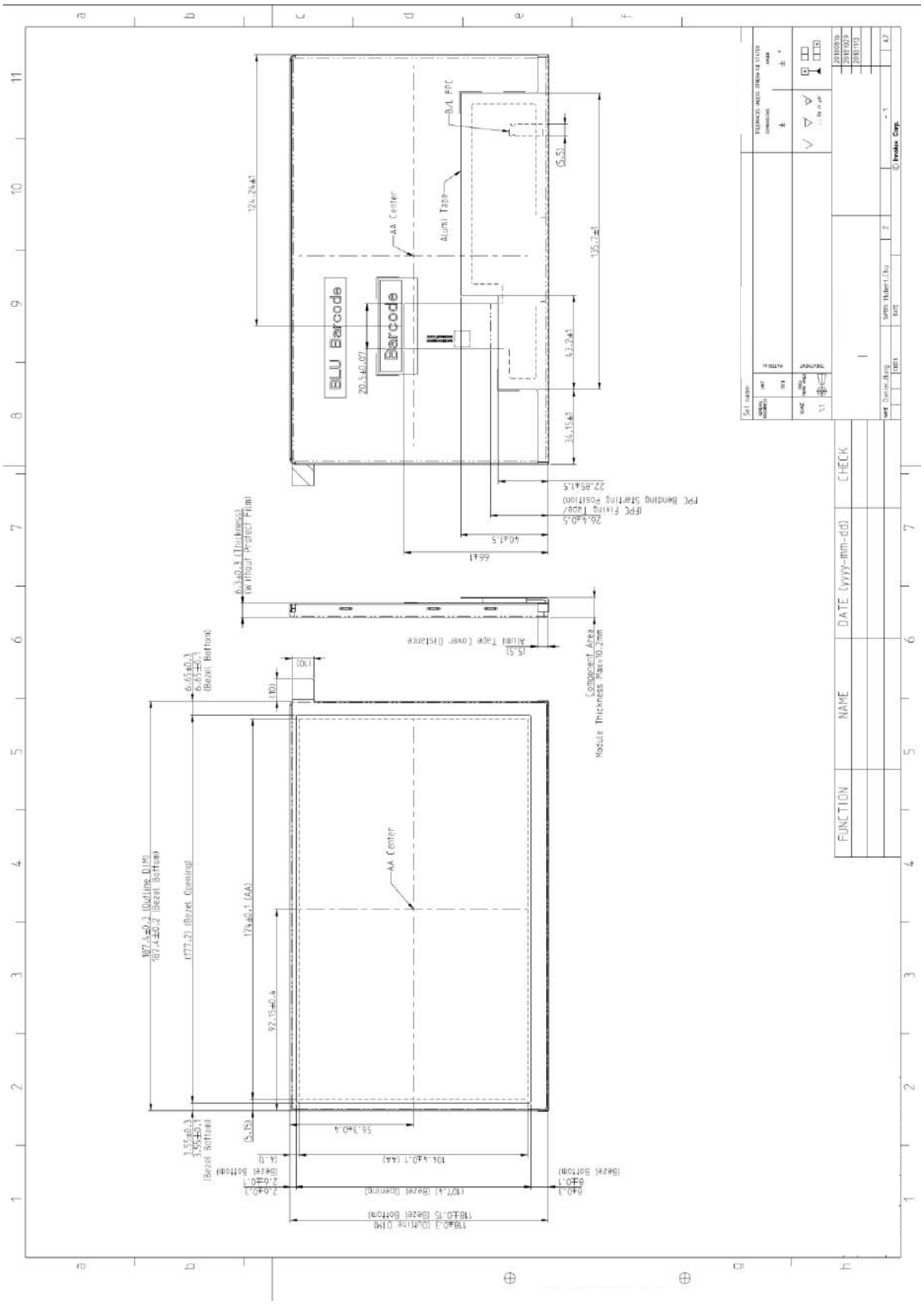
3. Store the module in an anti-electrostatic container or bag.

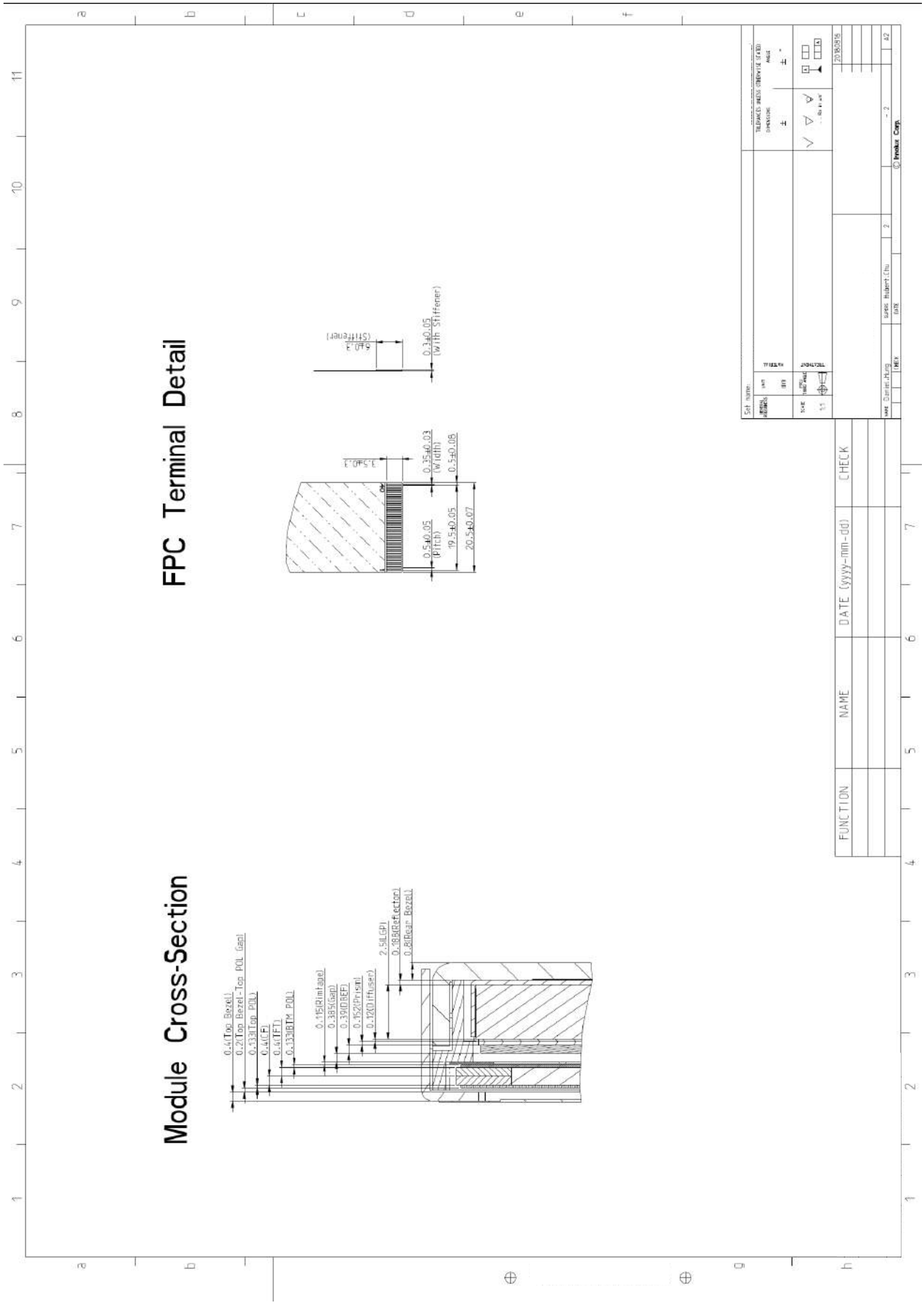
6.5 Cleaning

1. Do not wipe the polarizer with dry cloth. It might cause scratch.

2. Only use a soft sloth with IPA to wipe the polarizer, other chemicals might permanent damage to the polarizer.

7. Mechanical Drawing




FPC Terminal Detail
Module Cross-Section
0.4(Top Bezel)
0.2(Top Bezel-Top POL Gap)
0.133(Top POL)
0.4(CF)
0.4(TFT)
0.133(BTM POL)
0.115(Rimtape)
0.385(Gap)
0.39(DBEF)
0.152(Prism)
0.12(Diffuser)
2.5(LGP)
0.198(Reflector)
0.8(Rear Bezel)
0.3±0.05 (With Stiffener)
0.35±0.03 (Width)
0.5±0.08
0.5±0.05 (Pitch)
19.5±0.05
20.5±0.07
FUNCTION
NAME
DATE (yyyy-mm-dd)
CHECK