Product Specification

Model Name: TSO014VGHR-01

Description： 1.4” (454X454) AMOLED

Doc. Version： 01

Customer： Common Customers

■Approved for Preliminary Specification

□Approved for Final Specification

□Approved for Final Specification & Sample

Prepared	Checked	Approved

Customer’s Approval

Version History			
Version. No	Date	Contents	Remark

Contents

1 Scope

2 Features

2.1 Product Applications

Smart Watch

2.2 Product Features

1) Display color： 16.7M (RGB x 8bits)
2) Display format： 1.4”(454RGBx454)
3) Pixel arrangement： Real RGB arrangement
4) Interface： MIPI/SPI
5) Driver IC: RM69330

3 Maximum Rating

Parameter	Symbol	Spec			Unit	Note
		Min.	Typ.	Max.		
Analog/boost power voltage	VCI	-0.3	-	5.5	V	-
I/O voltage	VDDIO	-0.3	-	5.5	V	-
Operating temperature	Top	-20	-	60	℃	-
Storage temperature	Tstg	-30	-	70	℃	-

4 Mechanical Specifications

Item	Specification	unit
Dimension outline	38.83(V) x 38.21(W) x 0.68(T)	mm
LTPS Glass outline	38.83(V) x 38.21(W)	mm
Encapsulation Glass outline	ϕ38.21	mm
Number of dots	454(W) x RGB x 454(H)	dots
Active area	ϕ35.412	mm
Diagonal size	1.39	inch
Pixel pitch	78 x 78	μm
Glass thickness （LTPS/encapsulation glass）	0.2 / 0.2	mm
Weight	TBD	g

5 Electrical Specifications

5.1 Electrical Characteristics

5.1.1 Power Characteristic：

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
AMOLED Power positive	ELVDD	4.55	4.6	4.65	V	-
AMOLED power Negative	ELVSS	-2.45	-2.4	-2.35	V	Ref
Digital Power supply	VDDIO	1.65	1.8	3.3	V	Ref
Analog Power supply	VCI	2.7	2.8	3.6	V	Ref

1) Normal Mode

Power Supply: IOVCC=1.8V VCI=2.8V

Frame Frequency: F_{frame} =60HZ @ 25degC, Brightness 350 nits, Command Mode,

Display Condition	Symbol	Min.	Typ.	Max.	Unit	Remark
100% Pixel On 350nits	IELVDD /ELVSS	-	19.3	21.4	mA	Ref
	IVCI	-	6	7.2	mA	Ref
	IVDDIO	-	2	2.4	mA	Ref

2) Idle Mode

Power Supply: IOVCC=1.8V VCI=2.8V

Frame Frequency: F_{frame} =15HZ @ 25degC, Brightness:30nits, OPR:10%,Command Mode

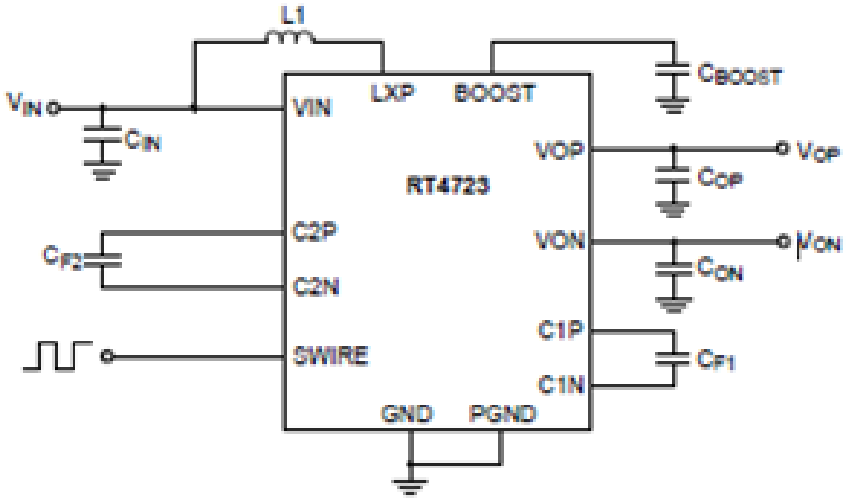
Display Condition	Symbol	Min.	Typ.	Max.	Unit	Remark
10% Pixel On 30 nits	IELVDD /ELVSS	-	-	-	mA	Supplied by Driver IC
	IVCI	-	3	3.6	mA	Ref
	IVDDIO	-	1.2	1.5	mA	Ref

3) Deep Standby Mode

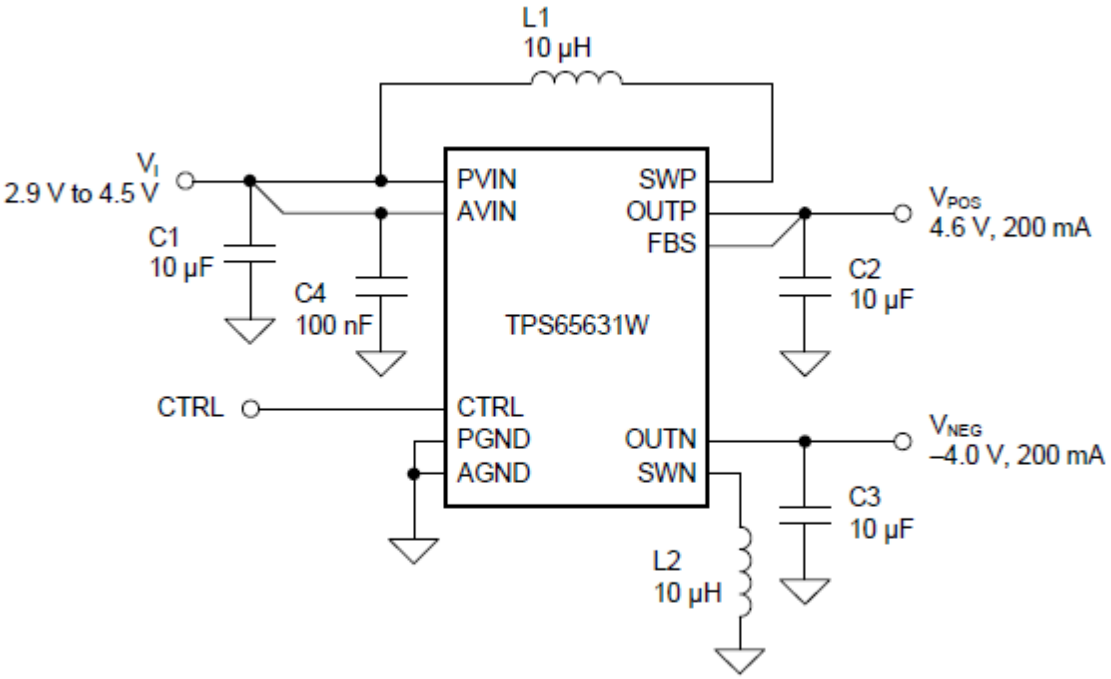
Display Condition	Symbol	Min.	Typ.	Max.	Unit	Remark
Deep Standby	IVCI	-	-	15	uA	-
	IVDDIO	-	-	4	uA	-
	Power Consumption	-	-	<50	uW	Ref

5.1.2 Power supply circuit application (This is for reference only)：

1) RT4723



2) TPS65631W

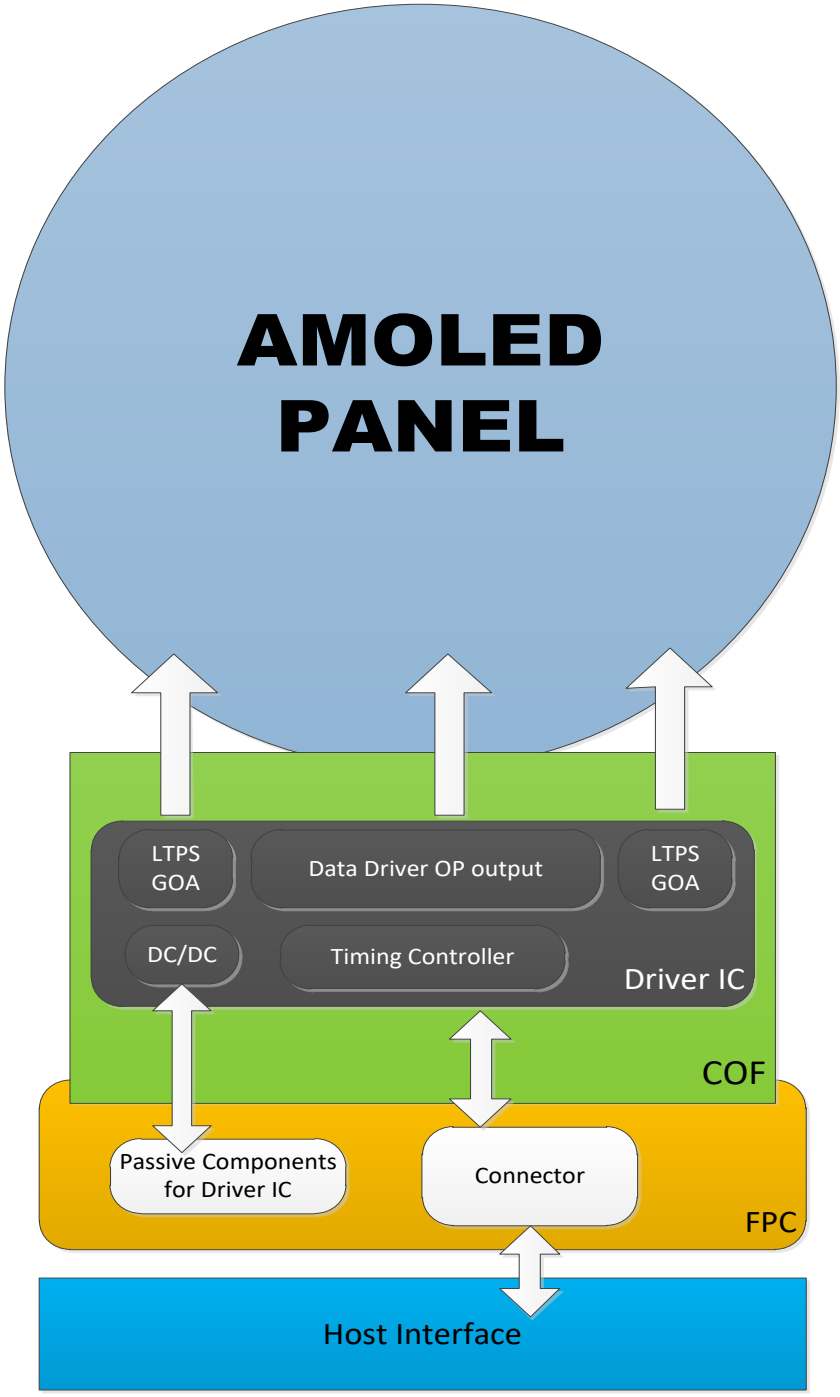


5.2 I/O Connection and Block Diagrams

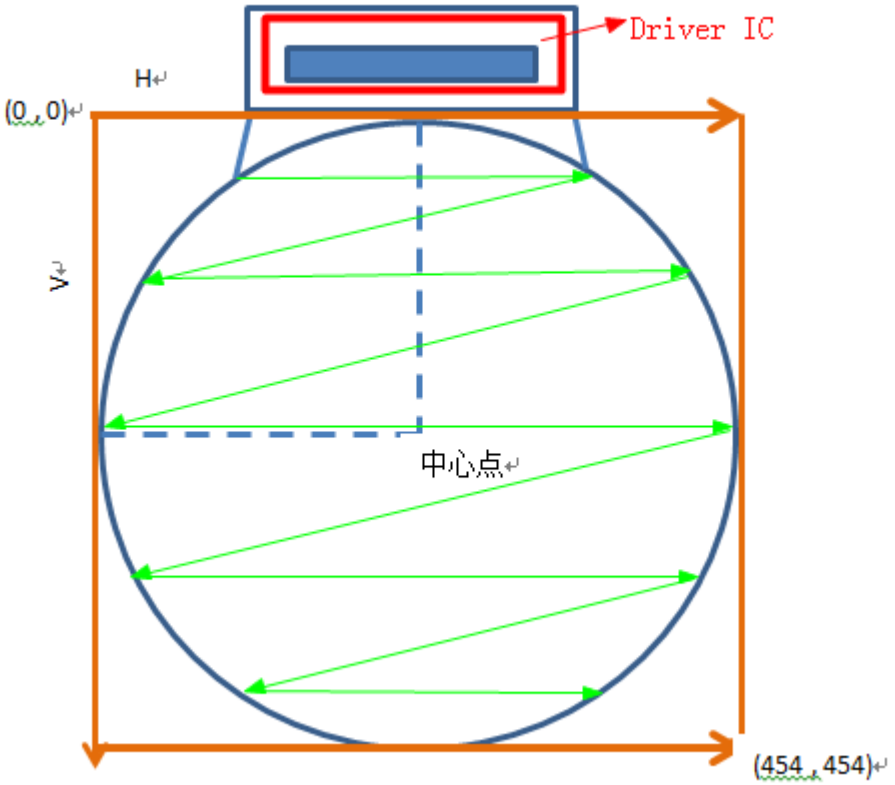
#	Pin name	I/O	Description
1	Reset	I	This signal will reset the device and must be applied to properly initialize the chip. Active low.
2	VCI_EN	I	This signal enables Power IC`s Driver IC analog supply
3	NC		
4	GND	Power	The power ground
5	TE	O	Tear effect output
6	DSI_D0N	I/O	MIPI DSI data0-
7	CSX	I	SPI Chip select input pin (“Low” enable)
8	DSI_D0P	I/O	MIPI DSI data0+
9	SCL	I	SPI Serial clock
10	GND	Power	The power ground
11	DCX	I	SPI CMD/Data selection signal
12	DSI_CLKN	I	MIPI DSI clock-
13	SDI	I	SPI input signal
14	DSI_CLKP	I/O	MIPI DSI clock+
15	SDO	O	SPI Output signal
16	GND	Power	The power ground
17	NC		
18	VDDI	Power	Driver IC digital I/O supply
19	VBAT	Power	Power IC supply
20	VDDI	Power	Driver IC digital I/O supply
21	VBAT	Power	Power IC supply
22	VBAT	Power	Power IC supply
23	VBAT	Power	Power IC supply
24	VBAT	Power	Power IC supply

5.3 Initial CODE

TBD

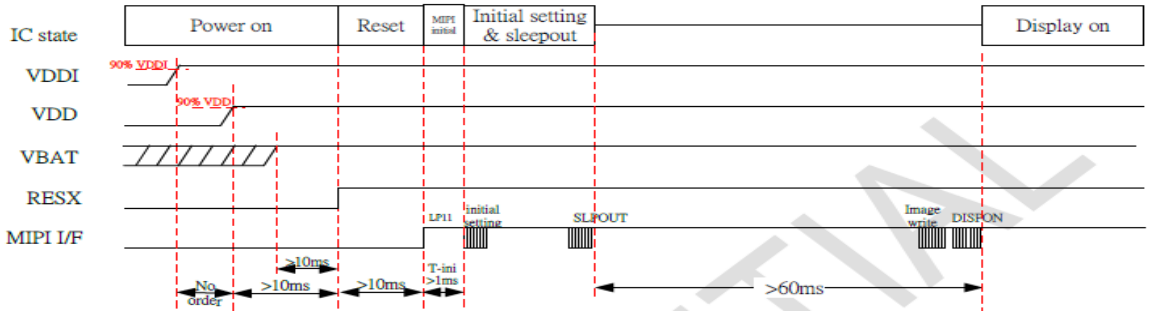

AMOLED
PANEL
LTPS
GOA
Data Driver OP output
LTPS
GOA
DC/DC
Timing Controller
Driver IC
COF
Passive Components
for Driver IC
Connector
FPC
Host Interface

5.4 Graphic memory writing direction

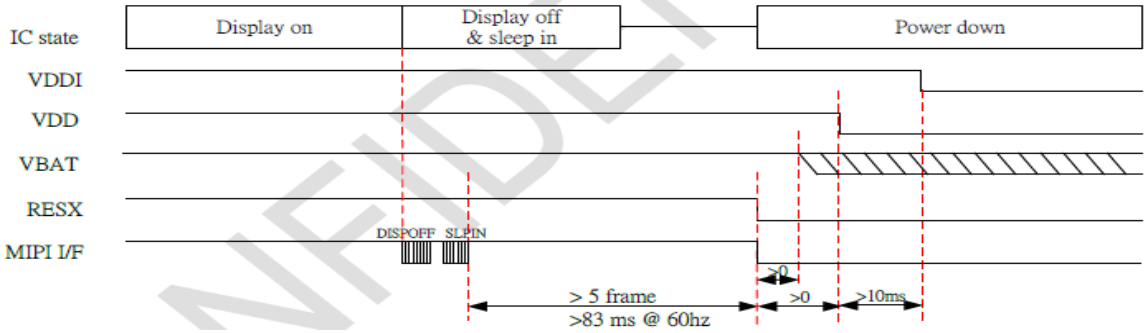


5.5 Recommended Operating Sequence

5.5.1 Power on sequence

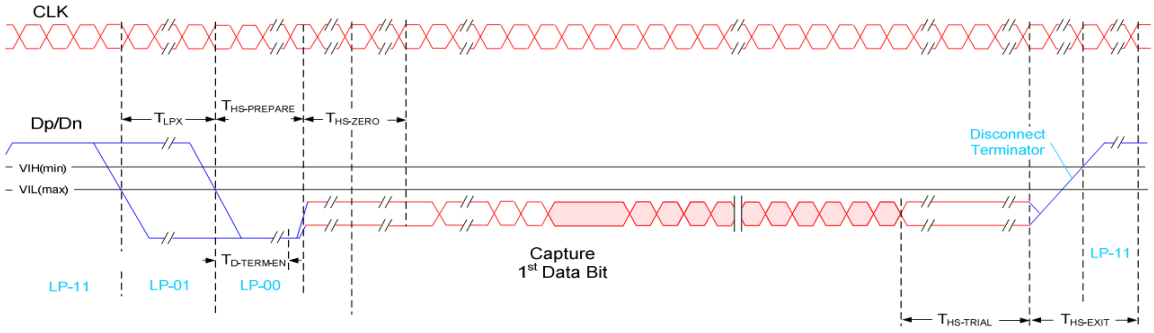


5.5.2 Power off sequence

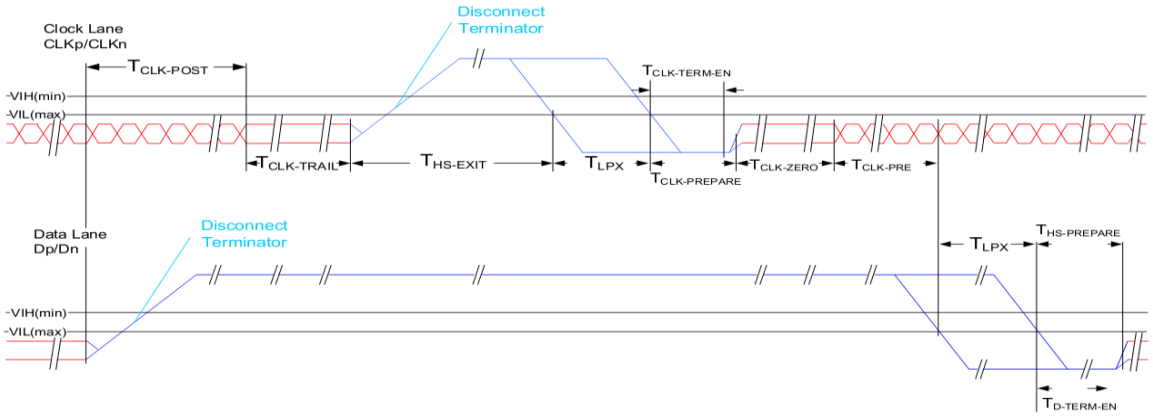


5.6 AC Characteristics（MIPI）

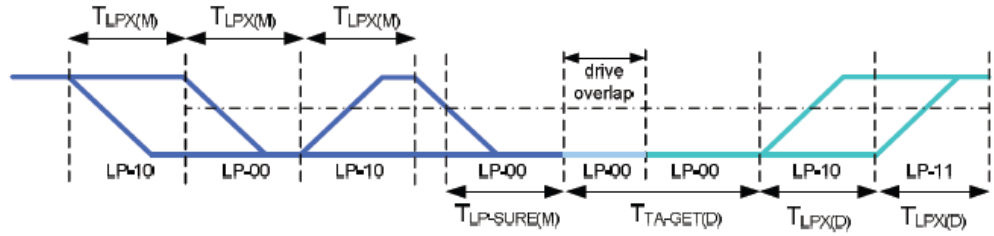
5.6.1 HS Data Transmission Burst



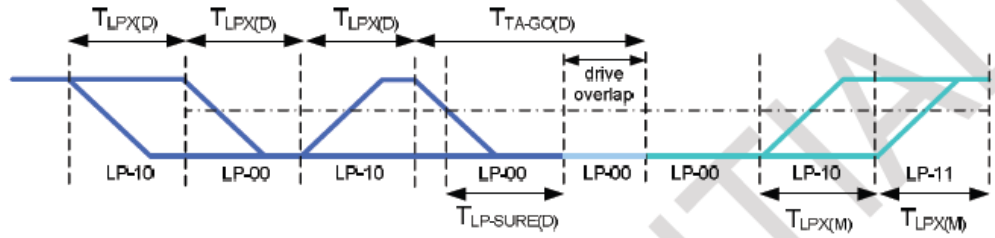
5.6.2 HS Clock Transmission



5.6.3 Turnaround Procedure



Bus turnaround (BAT) from MPU to display module timing



Bus turnaround (BAT) from display module to MPU timing

5.6.4 Timing Parameters

Symbol	Description	Min	Typ	Max	Unit
TREOT	30%-85% rise time and fall time	-	-	35	ns
TCLK-MISS	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.	-	-	60	ns
TCLK-POST*1	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of TCLK-TRAIL.	60ns + 52*UI (For DCS)	-	-	ns
TCLK-PRE	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8	-	-	ns

TCLK-SETTLE	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of TCLK-PRE.	95	-	300	ns
TCLK-TERM-EN	Time for the Clock Lane receiver to enable the HS line termination,starting from the time point when Dn crosses VIL,MAX.	Time for Dn to reach VTERM-EN		38	ns
THS-SETTLE	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of THSPREPARE.	85 ns + 6*UI		145 ns + 10*UI	ns
TEOT	Time from start of THS-TRAIL or TCLK-TRAIL period to start of LP-11 state	-	-	105ns+48*UI	ns
THS-EXIT(1)	time to drive LP-11 after HS burst	100	-	-	ns
THS-PREPARE	Time to drive LP-00 to prepare for HS transmission	40ns + 4*UI	-	85ns+6*UI	ns
THS-PREPARE + THS-ZERO	THS-PREPARE + Time to drive HS-0 before the Sync sequence	145ns + 10*UI	-	-	ns
THS-SKIP	Time-out at RX to ignore transition period of EoT	40	-	55ns+4*UI	ns
THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60 + 4*UI	-	-	ns
TLPX	Length of any Low-Power state period	50	-	-	ns

Ratio TLPX	Ratio of TLPX(MASTER)/TLPS(SLAVE) between Master and Slave side	2/3	-	3/2	ns
TTA-GET	Time to drive LP-00 by new TX	5*TLPX	5*TLPX	5*TLPX	ns
TTA-GO	Time to drive LP-00 after Turnaround Request	4*TLPX	4*TLPX	4*TLPX	ns
TTA-SURE	Time-out before new TX side starts driving	TLPX	-	2*TLPX	ns

5.6.5 Timing requirements for RESETB

When RESETB of the reset pin equals to Low, it will be in the condition of reset.

When it is in the condition of reset, it will make the device recover the initial set.

However, in order to avoid the reset noise cause reset, there is a mechanism to judge about whether the reset is needed or not.

The closed interval of Low can be shown as the following.

(Test condition: VDDIO=1.65V~3.6V, VSS=0V, T_A=-20℃~+70℃)

Parameter	Symbol	Conditions	Spec			Unit
			Min.	Typ.	Max.	
Reset low pulse width	Trst	-	20	-	-	μs

Table: Reset timing

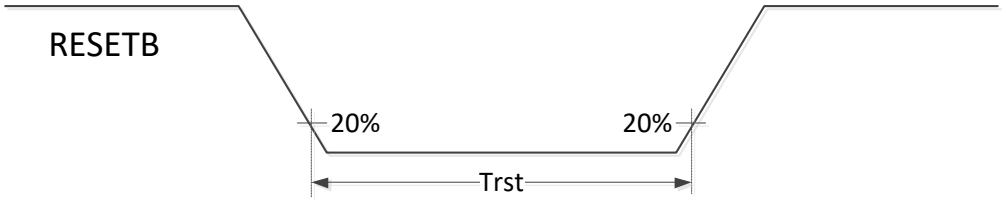


Figure: Reset timing

6 Electro-Optical Specification

Test condition： IOVCC=1.8V , VCI=2.8V ,Ta=25℃

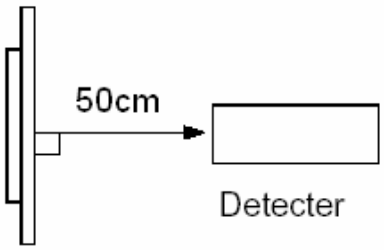
Item		Symbol	Condition	Value			Unit	Note
				Min	Typ	Max		
Luminance			θ=0°	315	350	385	cd/m2	Note 1
Uniformity			Φ=0°	85		-	%	Note 2
Viewing Angle	Left	θ_L	Cr≥200	80	85	-	Deg.	Note 3
	Right	θ_R		80	85	-		
	Top	ψ_T		80	85	-		
	Bottom	ψ_B		80	85	-		
Contrast Ratio		CR	θ=0°	5000	10000	-	-	Note 4

Response Time		Tr+Tf	Φ=0°	-	2	3	ms	Note 5
Color Coordinate of CIE1931	Red	X	θ=0° Φ=0°	0.636	0.676	0.716	-	-
		Y		0.283	0.323	0.363		
	Green	X		0.175	0.225	0.275		
		Y		0.68	0.73	0.78		
	Blue	X		0.103	0.143	0.183		
		Y		0.004	0.044	0.084		
	White	X		0.27	0.3	0.33		
		Y		0.28	0.31	0.34		
NTSC Ratio		NTSC	CIE1931	TBD	103	-	%	-
Flicker		-	-	-	-	-30	dB	-
Gamma		-	-	1.9	2.2	2.5		Note 6
Crosstalk		△CT	-	-	-	1.1		Note 7

Note 1: Luminance measurement

The test condition is measured on the surface of AMOLED module at 25℃.

- Measurement equipment CS2000 or similar equipment (Field of view:1deg,Distance:50cm)
- Measuring surroundings: Dark room.
- Measuring temperature: Ta=25℃.
- Adjust operating voltage to get optimum contrast at the center of the display.



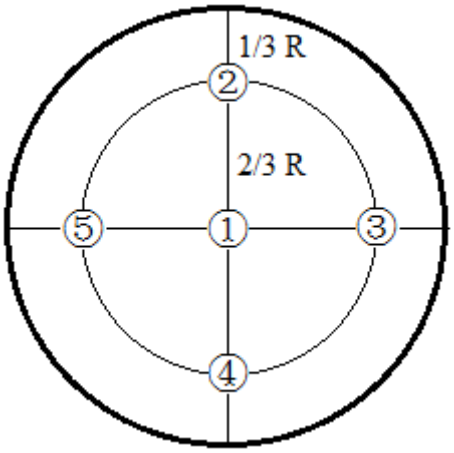
Note 2: Uniformity

The luminance uniformity is calculated by using following formula:

△Bp = Bp (Min.) / Bp (Max.)×100 (%)

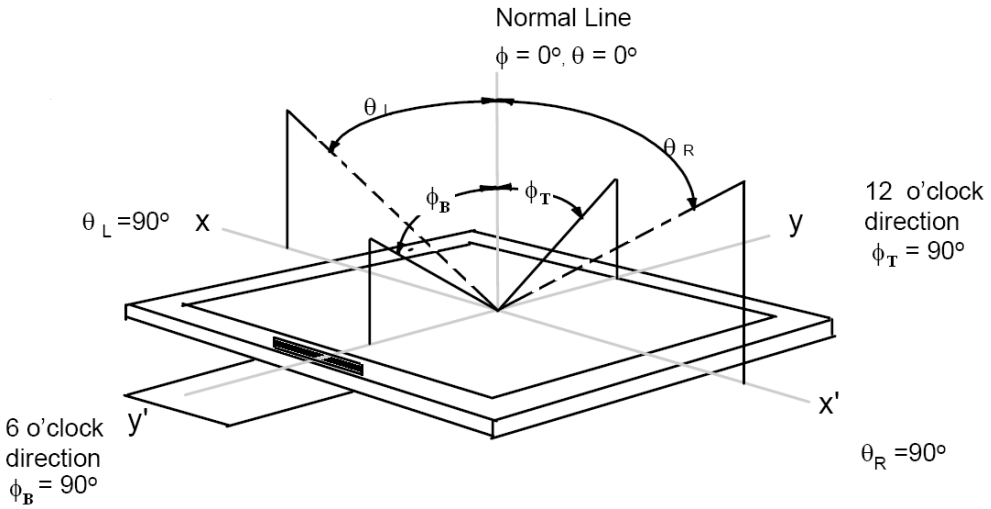
Bp (Max.) = Maximum brightness in 5 measured spots

Bp (Min.) = Minimum brightness in 5 measured spots.



Note 3: **The definition of Viewing Angle**

Refer to the graph below marked by ϑ and Φ

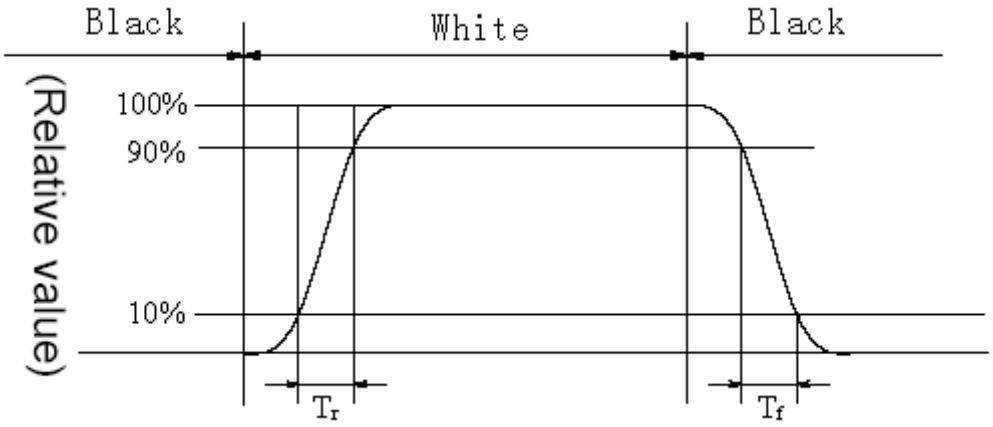


Note 4: **The definition of Contrast Ratio**:

$$\text{Contrast Ratio (CR)} = \frac{\text{Luminance When AMOLED is at “White” state}}{\text{Luminance When AMOLED is at “Black” state}}$$

Note 5: **Definition of Response time.**

The output signals of photo detector are measured when the input signals are changed from “black” to “white” (Voltage falling time) and from “white” to “black” (Voltage rising time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 6: Gamma curve

The whole curve's tolerance must control within +/-0.3, test the gray scale below:
8, 16, 25, 33, 41, 49, 58, 66, 74, 82, 90, 99, 107, 115, 123, 132, 140, 148, 156, 165, 173, 181, 189, 197,206, 214, 222, 230, 239, 255

Note 7: **Crosstalk**

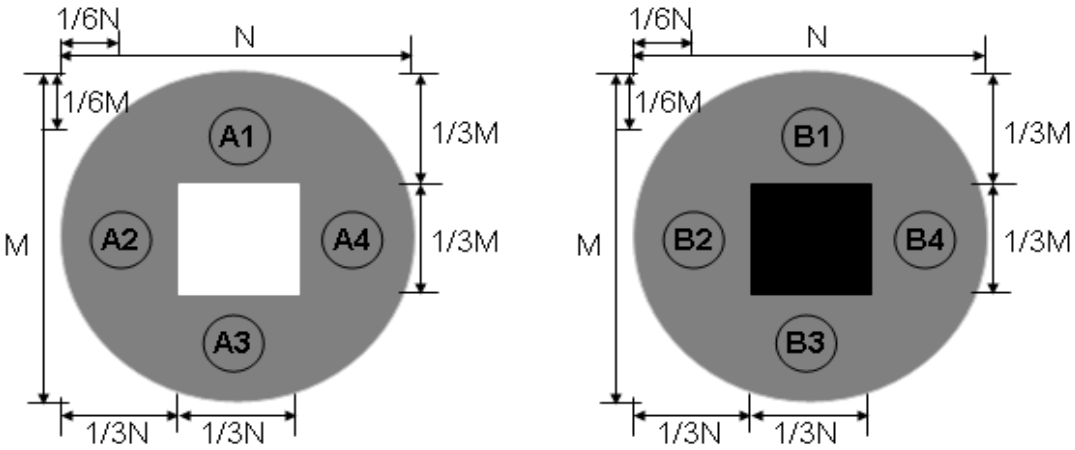
There should be no visible cross-talk in normal direction of the display when the two "Cross-talk Test Patterns" below are loaded.

△Bp (Max.) = Maximum value in △Bp1~△Bp4.

△Bp (Min.) = Minimum value in △Bp1~△Bp4.

△CT=△Bp (Max.)/ △Bp(Min.).

△CT must be less than 1.10



Cross-talk Test Pattern

7 Reliability

7.1 Environmental Test

Item	Main spec	No. of failures / No. of examinations
High Temperature Operation	70℃/ 128hours	0/ 5
Low Temperature Operation	-20℃/ 128hours	0/ 5
High Temperature Storage	80℃/ 128hours	0/ 5
Low Temperature Storage	-30℃/ 128hours	0/ 5
High Temperature Humidity Operation	60℃/ 90%RH 128hours	0/ 5
Thermal Shock	-40℃~80℃ 0.5hr, 30 cycles	0/ 5

7.2 Electrical Test

Item(Display)	Main spec	Note
Air Discharge	±4kV , 150pF/330Ω （Module level）	5Points, Each 2times. No degradation of OLED performance after this test.
Contact Discharge	±4kV, 150pF/330Ω （Module level）	

7.3 Mechanical Test

Item	Main spec	Note
Drop Test	Drop the packing from 75cm height, 3 times for 6-faces, 3-edges and 1-corner	Package
Vibration-proof test	2g, f=10->55->10Hz apply in each of X, Y, and Z direction for 30 min	Package

8 Handling Precautions

1. When cleaning ITO pad, avoid using hard and abrasive material or corrosive solution
2. Keep module away from direct sunlight or fluorescent light, and keep it at room temperature and humidity
3. Strong impact & pressure on module and packing is prohibited
4. Following normal power on/off sequence is necessary for preventing abnormal display or permanent damage to display
5. Optimal contrast ratio under ideal voltage is AMOLED module's characteristic, hence it is recommended a voltage control function available
6. Image sticking may occur if an image displays for an extended period of time
7. When interfered by system's overall mechanical design, an abnormal display may occur
8. After considering emitting energy, you should plan your design to satisfy EMI standards.
9. Host side should place a surge-prevent circuit at power trace (ie: VCI, Vddi) to protect AMOLED module.

9 Outline Dimension Drawing

TBD

10 The Control of Hazardous substances